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48154 7590 10/28/2005

SLATER & MATSIL LLP
17950 PRESTON ROAD
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Kristin R. Hayes	(Depositor's name)
<i>KR Hayes</i>	(Signature)
January 16, 2006	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,128	02/13/2004	Till Schloesser	INF-135	3801

TITLE OF INVENTION: METHOD OF FABRICATING AND ARCHITECTURE FOR VERTICAL TRANSISTOR CELLS AND TRANSISTOR-CONTROLLED MEMORY CELLS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$1700	01/30/2006
EXAMINER	ART UNIT		CLASS-SUBCLASS		
HUYNH, ANDY	2818		257-302000		

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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2. For printing on the patent front page, list

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PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Infineon Technologies AG

Munich, Germany

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

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 A check in the amount of the fee(s) is enclosed. Payment by credit card. Form PTO-2038 is attached. The Director is hereby authorized to charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-1063 (enclose an extra copy of this form).

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 a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Authorized Signature *[Signature]*

Date January 16, 2006

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FACSIMILE COVER SHEET

To: Commissioner for Patents	Total Pages Sent: 3
Mail Stop Issue Fee	(including cover sheet)
Facsimile Number: (571) 273-2885	Transmission Date: January 16, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Schloesser, et al. Docket No.: INF-135
 Serial No: 10/777,128 Art Unit: 2818
 Date Filed: February 13, 2004
 Title: Architecture for Vertical Transistor Cells and Transistor-Controlled Memory Cells

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at (571) 273-2885 on the date shown above:

- Certification of Facsimile Transmission (1 page)
- Part B - Fee Transmittal (2 duplicate pages)

Respectfully submitted,

Kristin R. Hayes
 Legal Assistant

Confirmation Respectfully Requested

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